WHAT IS CLAIMED IS:

1. A digital embedded architecture, including a microcontroller and a memory device, suitable for reconfigurable computing in digital signal processing and comprising: a processor, structured to implement a Very Long Instruction Word elaboration mode by a general purpose hardwired computational logic, and an additional data elaboration channel comprising a reconfigurable function unit based on a pipelined array of configurable look-up table based cells controlled by a special purpose control unit.

2. A digital embedded architecture according to claim 1, wherein said reconfigurable function unit includes a hardware-based Field Programmable Gate Array (FPGA) embedded devices.

3. A digital embedded architecture according to claim 1, wherein said additional data elaboration channel is tightly integrated in a processor core, receiving inputs from a register file and writing results on dedicated write back channels over the register file.

4. A digital embedded architecture according to claim 1, wherein said pipelined array of configurable lookup-table based cells implements a configurable run-time with a variable latency data path capable to emulate a potentially infinite number of virtual application specific function units.

5. A digital embedded architecture according to claim 4, wherein the architecture is based on three different and concurrent data elaboration flows, two of which feed each cycle by instruction fetch and one based on an independent, variable latency pipeline implemented on the configurable data-path.

6. A digital embedded architecture according to claim 2, wherein said configurable gate-array is a Pipelined-Configurable-Array (PiCo-Array) comprising a pipelined array of configurable lookup-table based cells virtually emulating a microprocessor data path.

7. A digital embedded architecture according to claim 6, wherein the cells of said PiCo-Array structure are grouped in rows, each representing a possible stage of a customized pipeline, and the whole array can be represented by a control data flow graph, each row or group of rows corresponding to a different state.

8. A digital embedded architecture according to claim 3, wherein at any decoded instruction of the pipelined array a corresponding destination register file is locked, so that any following instruction trying to access such a register will cause a processor stall; normal execution being restored only when the pipelined array completes the write-back operation unlocking its destination register.

9. A digital embedded architecture according to claim 3, wherein said special purpose control unit is a hardwired, run-time programmable Data-Flow-Graph based control unit synchronizing the pipelined computation of the gate-array cells.

10. A digital embedded architecture according to claim 8, wherein the locking mechanism of said register file supports the highest possible level of resource utilization parallelism allowing unpredictable latency instructions to be executed on the configurable unit without altering program flow consistency.

11. A digital embedded architecture according to claim 3, wherein said register file comprises four read ports, used to support the issue of two RISC instructions each clock cycle, and two write ports reserved for said two hardwired pipeline channels; two other ports being entirely dedicated to write back results of the pipelined array, thus avoiding introduction of dedicated logic handling competition on the register file ports.

12. A digital embedded architecture according to claim 1, wherein said pipelined array comprises a first level cache, storing four configurations for each logic cell; and further comprising a context switch for taking only one clock cycle and providing four immediately available instructions.

13. A digital embedded architecture according to claim 1, further comprising a specific extension of the instruction set architecture for controlling configuration and

execution over the configurable array, said instruction set architecture including 32-bit and 64-bit instructions taking advantage of the entire VLIW instruction word.

14. A digital embedded architecture according to claim 1, further comprising a special purpose reconfiguration mechanism for allowing very fast configuration completely concurrent with processor execution, said reconfiguration mechanism including the configurable array being structured in blocks, having at least eight rows each, each block being reprogrammed while the other blocks are under execution.

15. A circuit, comprising:

a processor configured to implement a plurality of concurrent data elaboration flows;

a programmable logic device coupled to the processor and performing a data elaboration function; and

a control device coupled to the logic device and controlling operation of the logic device.

16. The circuit of claim 15, wherein the logic device comprises a hardware-based Field Programmable Gate Array.

17. The circuit of claim 15, wherein the logic device comprises a pipelined array of configurable lookup-table based cells emulating a microprocessor data path.

18. The circuit of claim 15, wherein the logic device implements a configurable run-time with a variable latency data path.

19. The circuit of claim 17, wherein the control device synchronizes the pipelined computation of the gate-array cells.

20. A computer system, comprising:

a memory device; and

a semiconductor chip, comprising:

a processor configured to implement a plurality of concurrent data elaboration flows;

a programmable logic device coupled to the processor and performing a data elaboration function; and

a control device coupled to the logic device and controlling operation of the logic device.

21. A method of algorithmic data elaboration, comprising:

employing a processor to elaborate a first portion of the algorithmic data;

employing a programmable logic device coupled to the processor to elaborate a second portion of the algorithmic data, operation of the logic device being controlled by a control device.

22. The method of claim 21, wherein the logic device comprises a pipelined array of configurable lookup-table based cells emulating a microprocessor data path.

23. The method of claim 21, wherein:

employing a processor comprises writing data to a register file over a first port dedicated to the processor; and

employing a programmable logic device comprises writing data to the register file over a second port dedicated to the logic device.

24. The method of claim 23, wherein employing a programmable logic device further comprises:

decoding a logic device instruction; and

locking a destination register of the register file in response to decoding the logic device instruction, the destination register corresponding to the instruction.

25. The method of claim 24, wherein employing a programmable logic device further comprises unlocking the destination register in response to writing data to the register file over the second port.